

I hereby certify that this correspondence was deposited with the United States Postal Service as first class mail in an envelope addressed to:

PATENT  
Attorney Docket No.: 015114-047930US  
Client Reference No.: A293-D1

Assistant Commissioner for Patents  
Washington, D.C. 20231

TOWNSEND and TOWNSEND and CREW LLP

By:

*July 5, 2001*

*James Cassin Can*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Raminda U. Madurawe et al.

Application No.: 09/606,252

Filed: June 28, 2000

For: HIGH VOLTAGE MOS DEVICES  
WITH HIGH GATED-DIODE  
BREAKDOWN VOLTAGE AND  
PUNCH-THROUGH VOLTAGE

Examiner: Paul E. Brock II

Art Unit: 2815

AMENDMENT

RECEIVED  
JUL 17 2001  
TC 2800 MAIL ROOM

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

In response to the Office Action mailed January 5, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 27-28, and 35-37 as indicated below and in the attachment.

Please add new claims 38-40.

- 1 *Sub C1* 27. (Amended) A method of fabricating a transistor in an integrated circuit  
2 device comprising:  
3 *21* providing a semiconductor substrate;  
4 forming a gate oxide on the semiconductor substrate;  
5 forming a gate on the gate oxide;